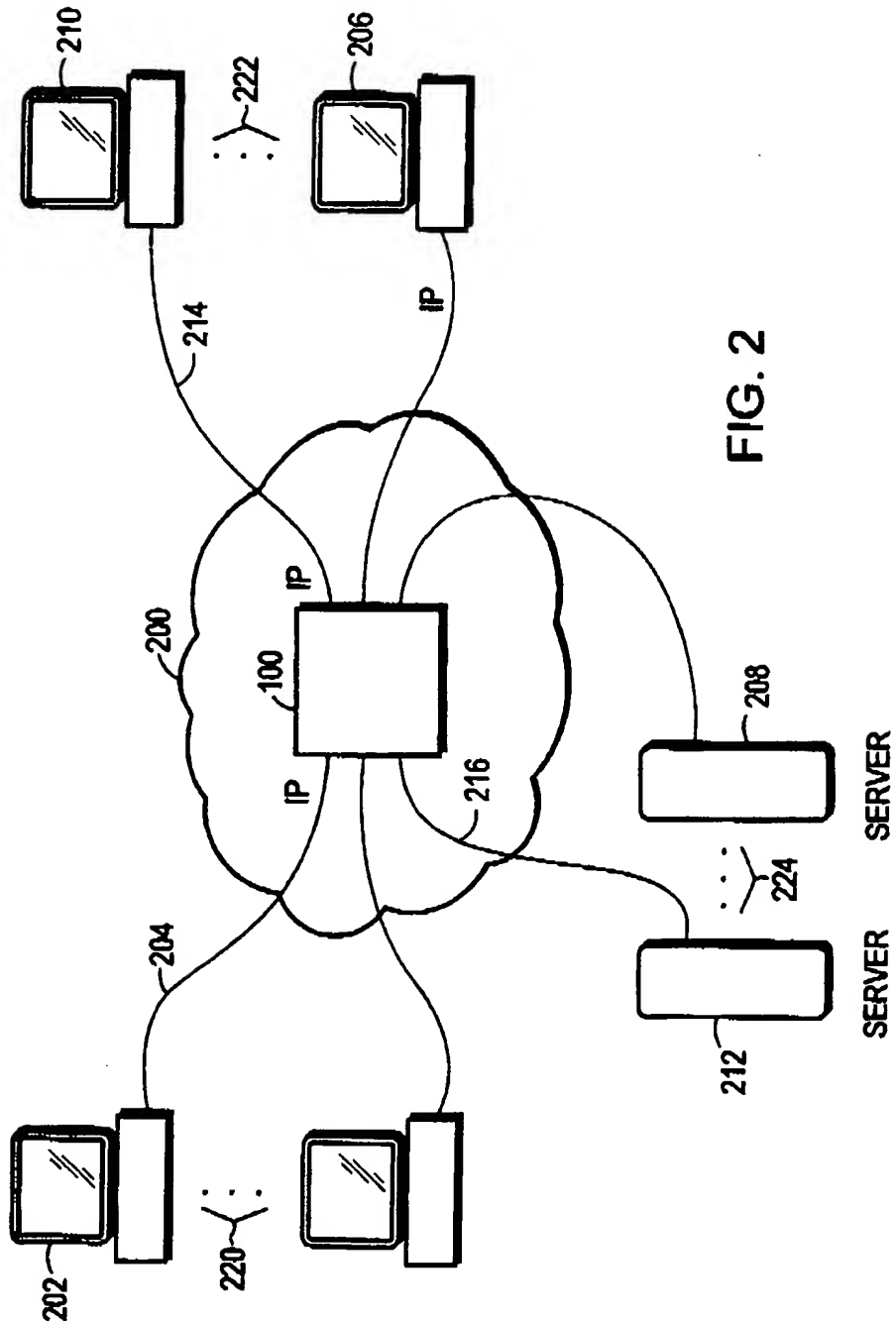


SWITCH WITH LINECARDS QUEUES, AND THRESHOLDS

FIG. 1



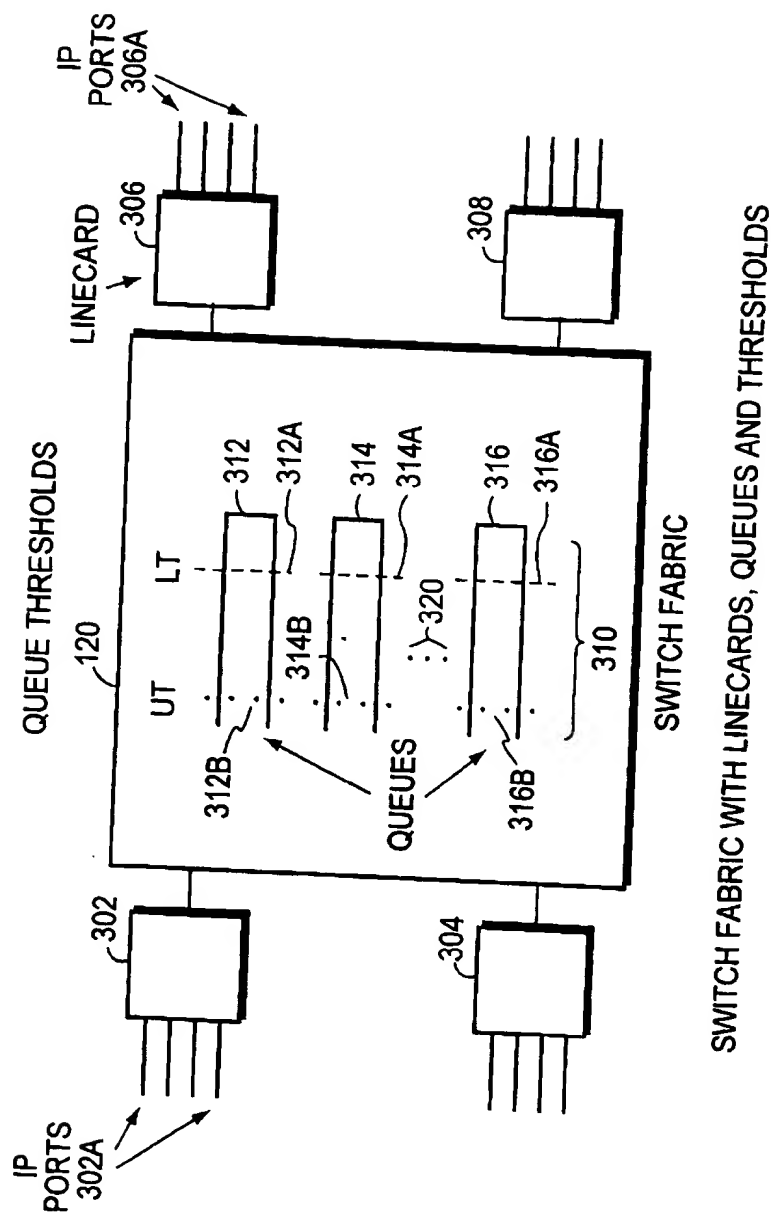
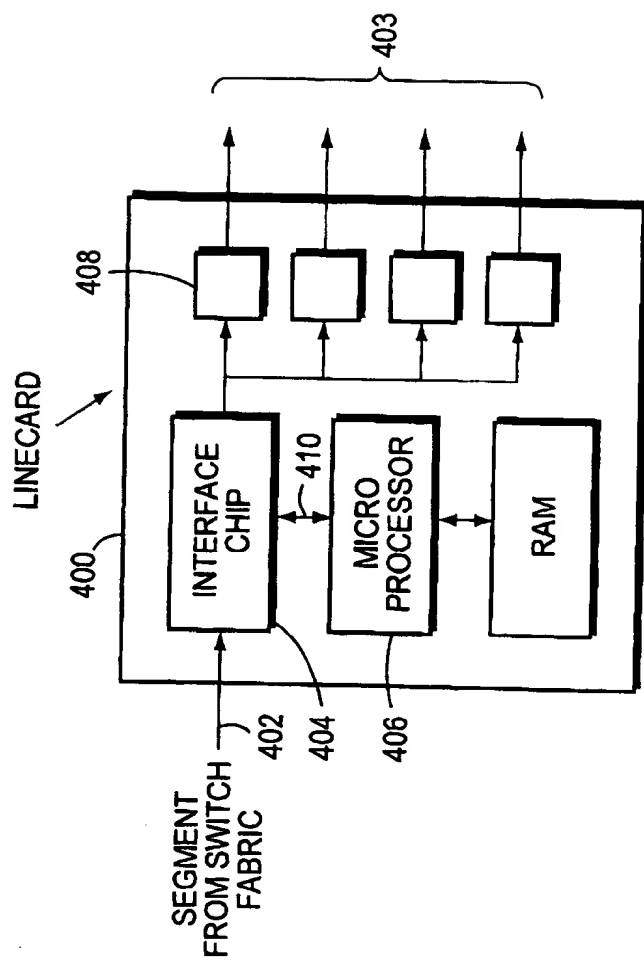


FIG. 3

+



LINECARD WITH MICRO-PROCESSOR FOR EXECUTING RED ALGORITHM,
RAM MEMORY FOR STORING CODE AND DATA

FIG. 4

+

[illegible]

ATM CELL STRUCTURE



⌊

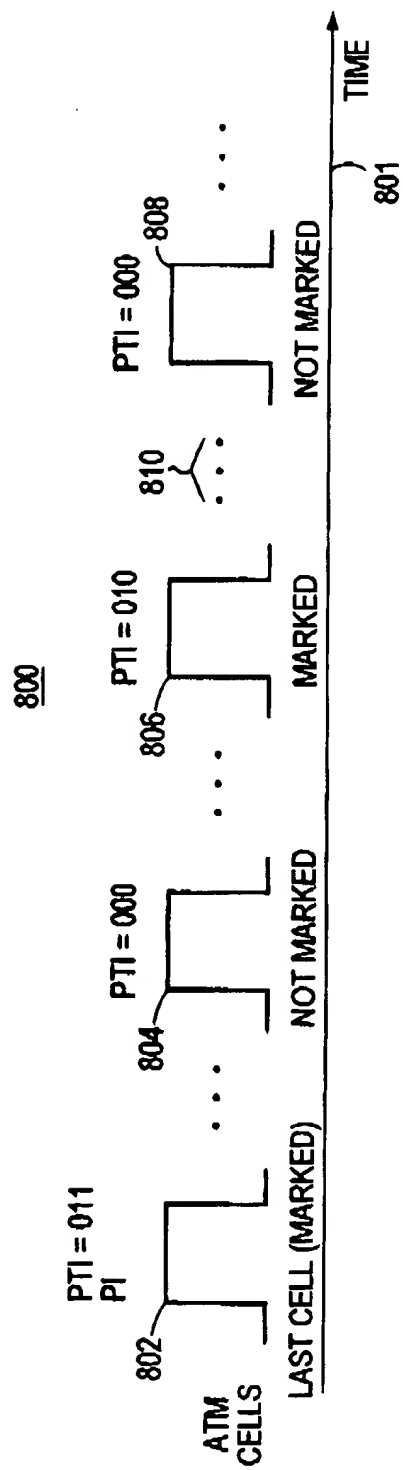


FIG. 8

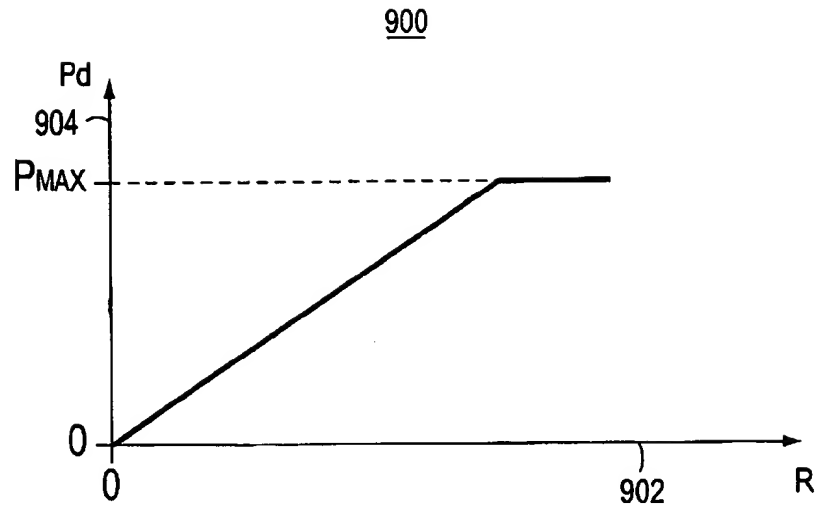
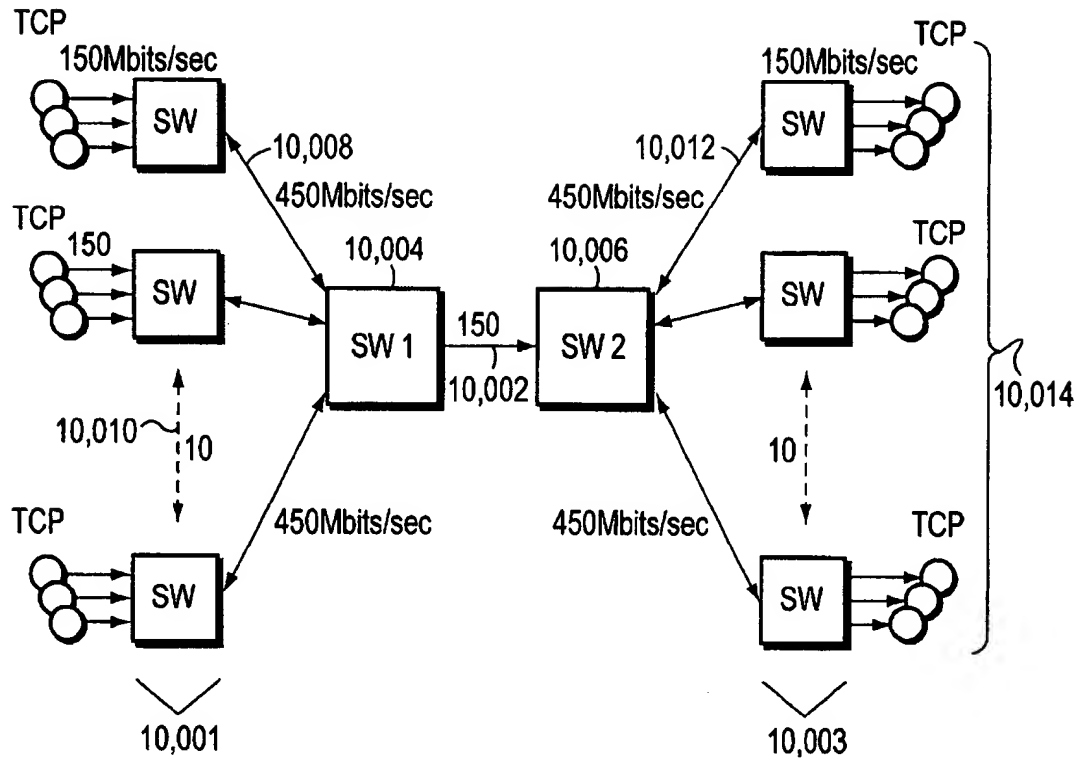


FIG. 9

000201-6T4E960



TOPOLOGY FOR RED SIMULATIONS

FIG. 10

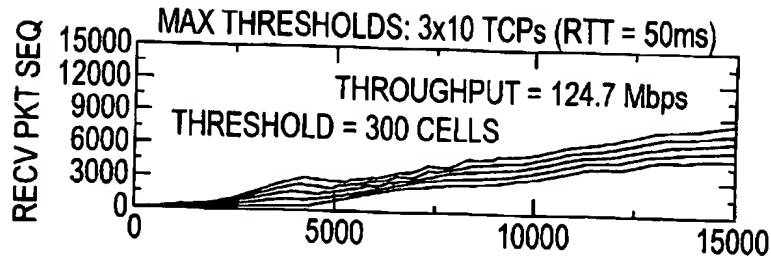


FIG. 11A

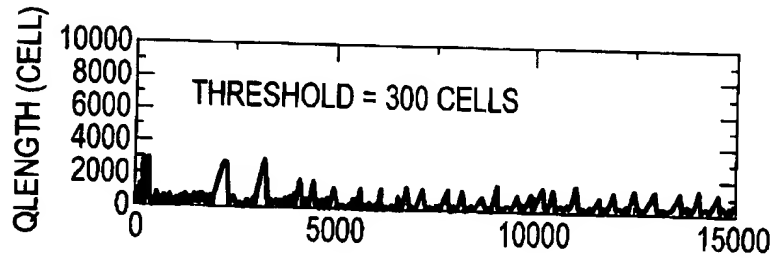


FIG. 11B

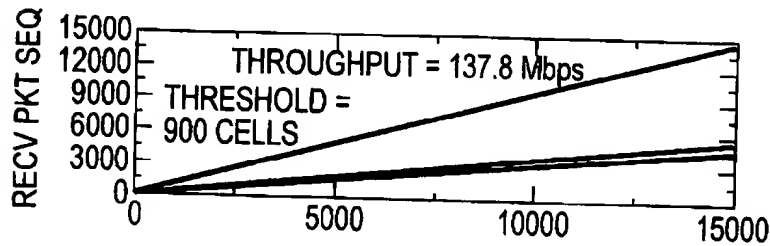


FIG. 11C

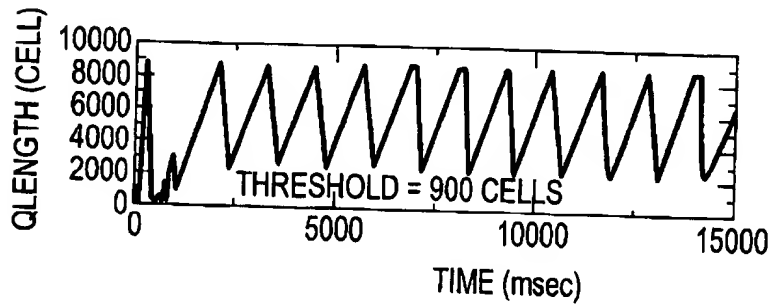


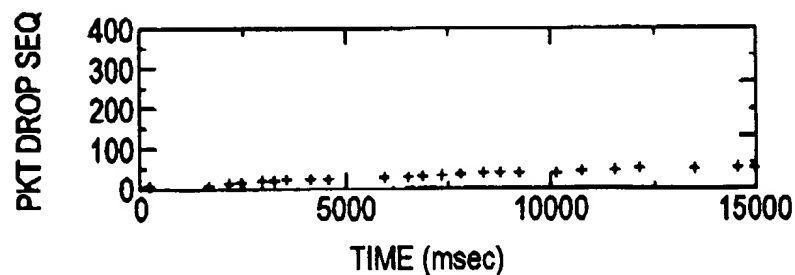
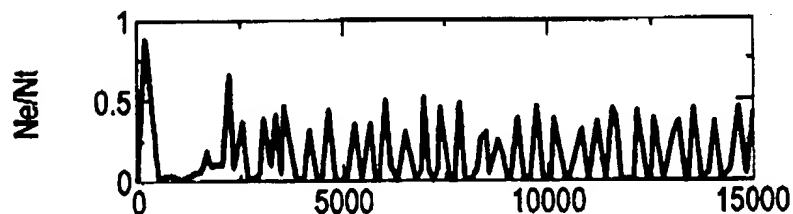
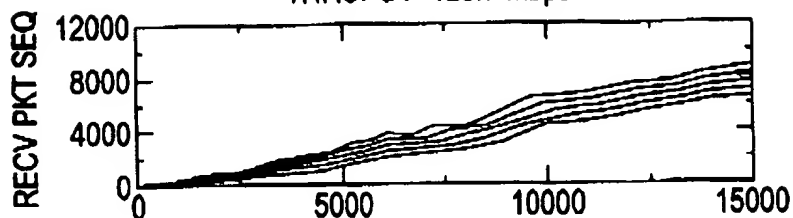
FIG. 11D

RESULTS FOR EPD-THRESHOLD = 300, 900

000007 6746960

10/13

RED: 3x10 TCPs (RTT = 50ms)
Qth=100/300; MAXP=0.01; FREEZE=100ms;
THRUPUT=128.7 Mbps



RESULTS FOR EFCI-THRESHOLD = 100,
EPD = 300

000007-6746960

RED: 3x10 TCP (RTT = 50ms)
 Qth=300/900; MAXP=0.01; FREEZE=100ms;
 THRUPUT=137.2 Mbps

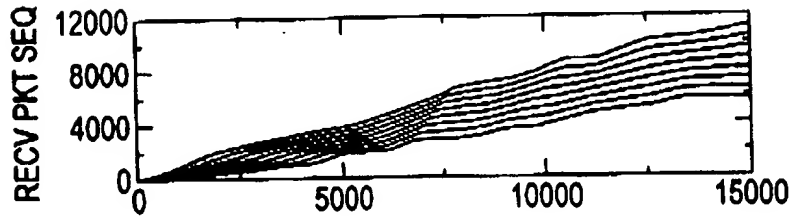


FIG. 13A

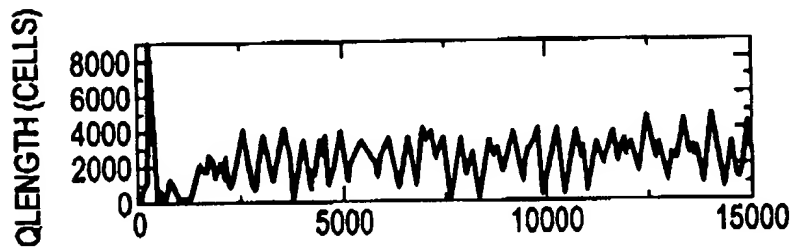


FIG. 13B

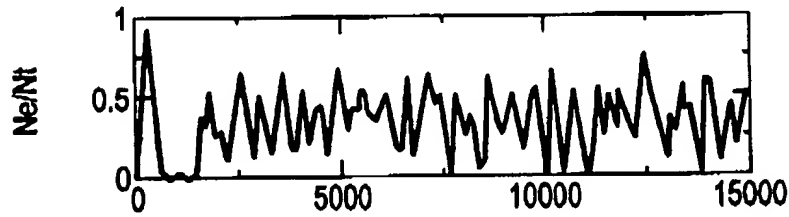


FIG. 13C

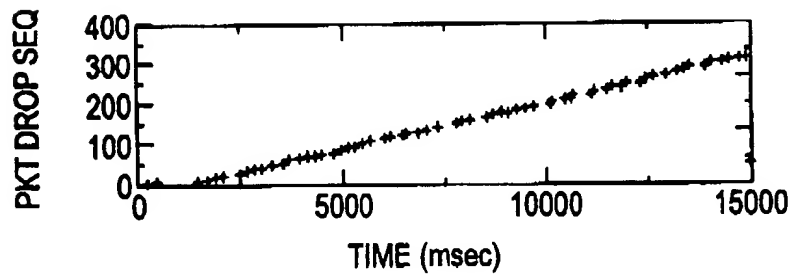


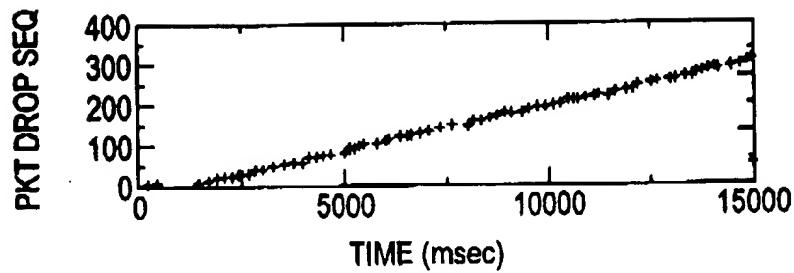
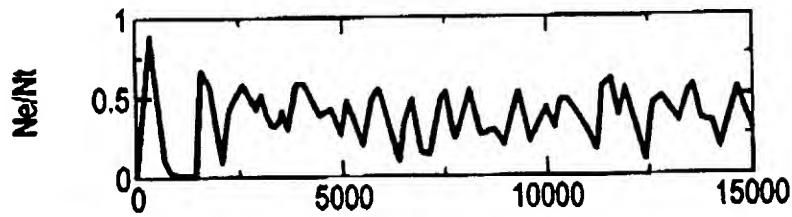
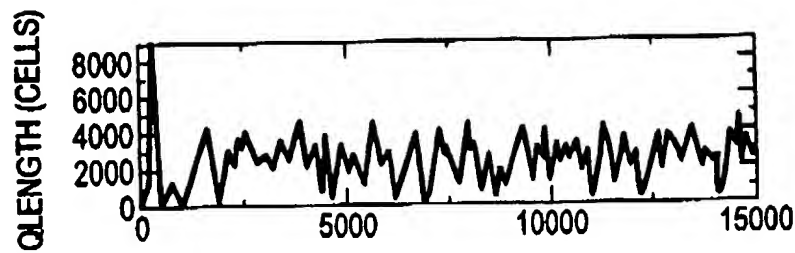
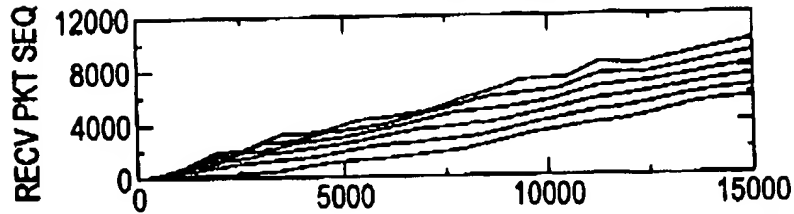
FIG. 13D

RESULTS FOR EFCI-THRESHOLD = 300,
 EPD = 900

000001 = 6746960

12/13

RED: 3x10 TCP (RTT = 50ms)
Qth=300/900; MAXP=0.01; FREEZE=200ms;
THRUPUT=137.3 Mbps



RESULTS FOR PD UPDATE INTERVAL = 200 msec

000001-6746960

RED: 10/20 (Hi/Lo) TCPs (RTT = 50ms)
 PER-CLASS VS. PER-CLASS PER-PREF RATIOS; MAXP=1.0/2.0%

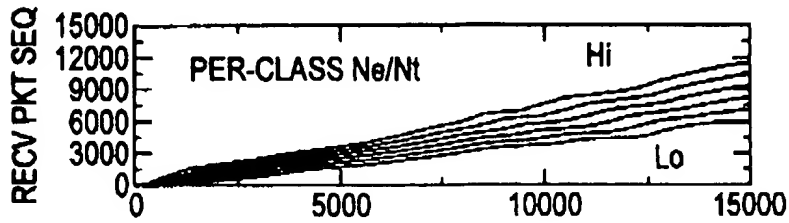


FIG. 15A

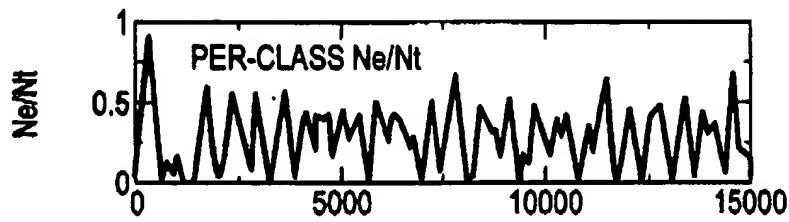


FIG. 15B

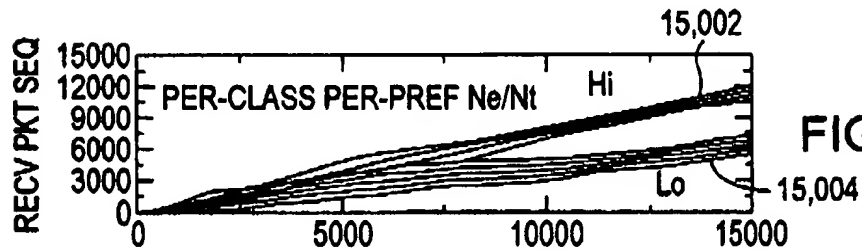


FIG. 15C

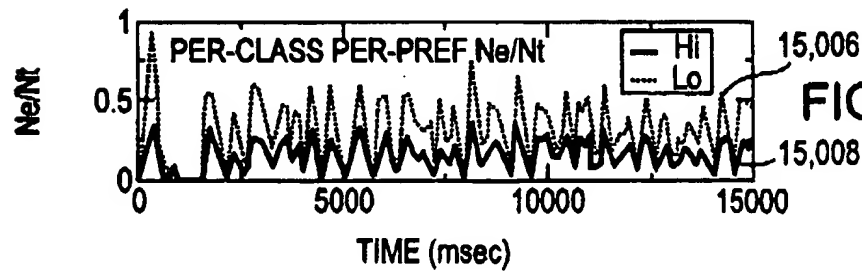


FIG. 15D

PER-CLASS VS. PER-CLASS PER-PREFERENCE Ne/Nt

000001-01426960